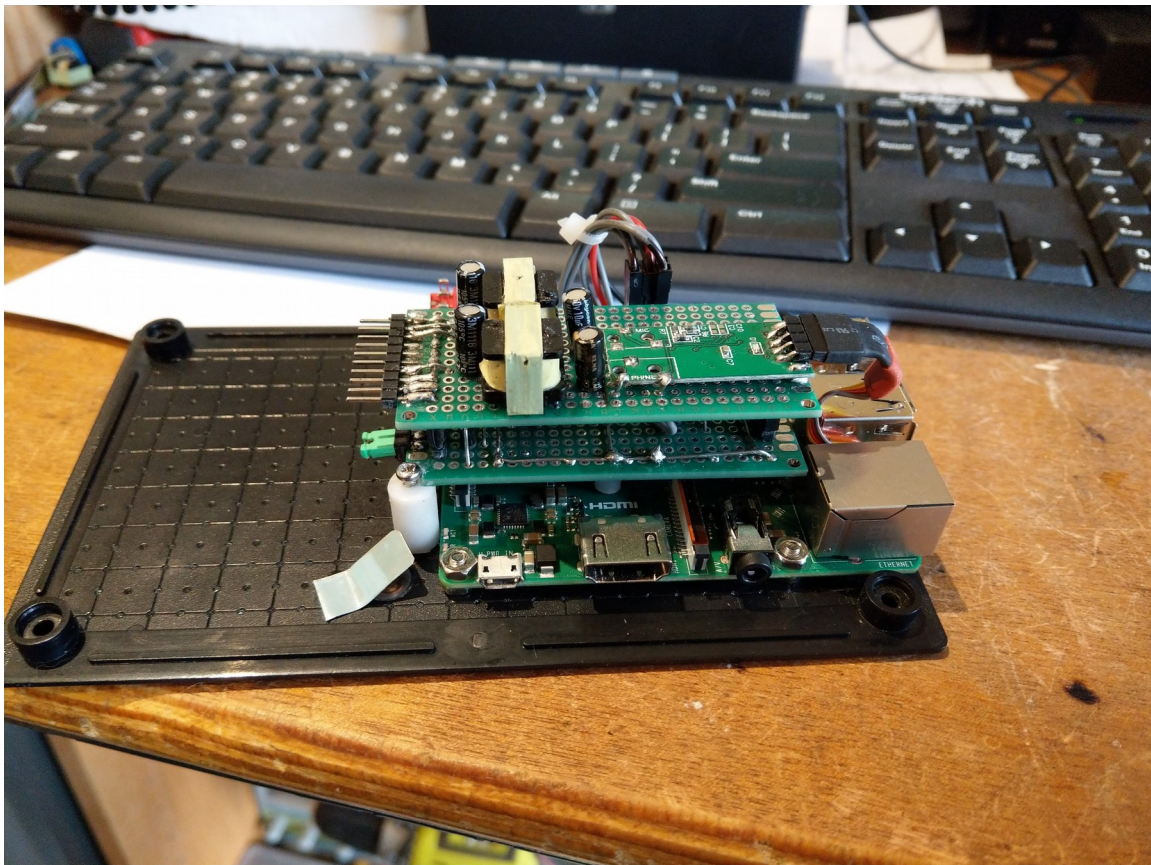


## IRLP Node for Raspberry Pi

The motivation behind this new NODE design was driven by the cost of purchasing from the developer (David Cameron (VE7LTD)), to be a very expensive exercise, due to our exchange rate.

David did develop software for his board to be used on a Raspberry Pi, resulting in a compact neat stand alone node device, the down side is that he uses the same PCB that he developed for his long time standing PC system

Getting involved with the Victorian Repeater Linking project, the need arose to develop a new kind of IRLP Node, to be used for repeater linking projects, that could not be done using RF technology.



Vero Board Prototype

The design parameters, required that the IRLP Logic and Audio circuits be built on a hat that would sit on top of the Raspberry Pi, have the ability to take care of itself during system failures with the ability to recover without human intervention, (self healing), this required some modifications to the original IRLP code along with hardware changes, deviating from the original IRLP hardware design.

In the original, there is provision for Auxiliary ports, I have done away with these, as they serve no purpose for the intended application as a repeater link, but the original I/O pins and software are retained, should these be required in the future.



Completed prototype

On cold start, the node is designed to connect to a selected host reflector ( Home), on no activity, or in a power fail recovery.

Using the onboard hardware watchdog, the node is also able to determine if the internet is viable and functional, should this not be the case the node will retry to connect to the Home host. (Presently there is no limit to the number retries.)

External supervisory LED's have been included to the hardware with the required software changes to implement this, as an aid to indicate activity such as PTT, Valid DTMF , COS, SD access and Link Active.

SD card corruption is a concern, usually caused by improper CPU shutdown, even if using prime quality SD cards such as Sandisk, corruption is possible under some conditions, code was developed by VK3NA that upon a power down or power fail the Node will do a proper shut down procedure. In hardware this is possible by using a back up power supply that uses a super capacitor as the power source, this having sufficient energy for proper shutdown of the Raspberry CPU.

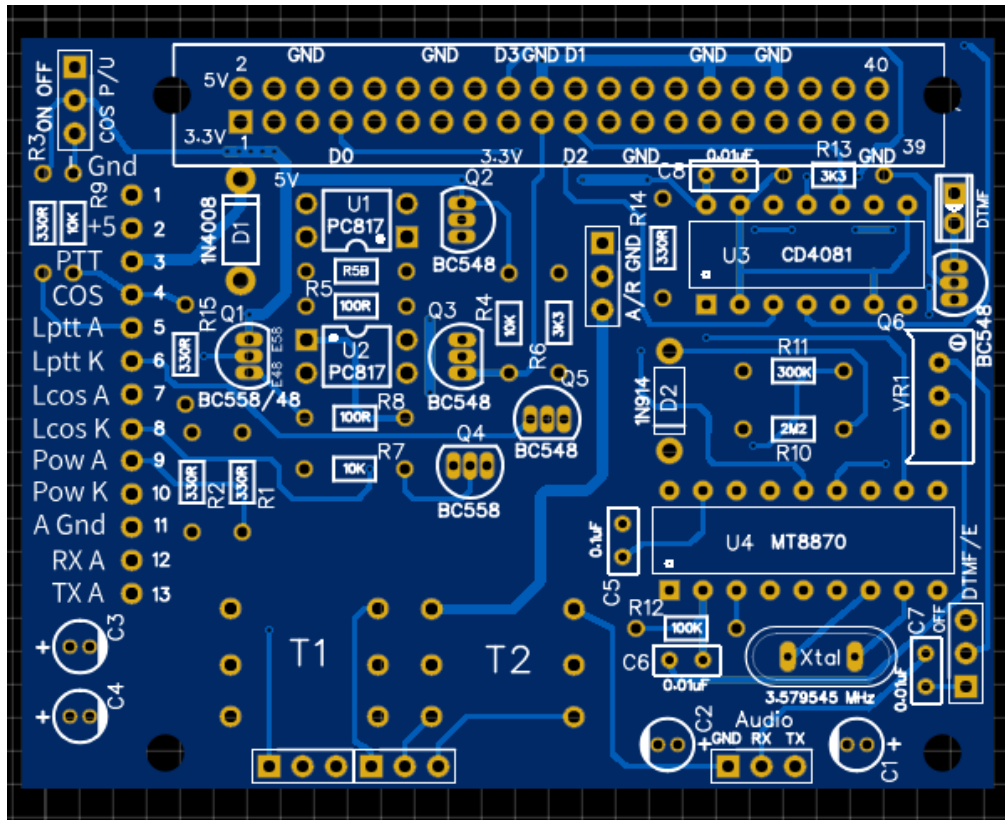
VK3NA developed code that indicates if the node is connected to a host or not, indicated by the Link Active LED.

The Node uses audio decoupling transformers and opto-couplers, for radio control, the aim was to reduce unwanted noise achieving the best possible audio quality, providing protection to the Raspberry Pi Computer.

One of the weakness of the Raspberry Pi, is the 3 Volt onboard regulator, this is easily damaged, I chose to only use 5 Volts with current limiting on the I/O channels, a benefit is that the board will work with radios that use 3.3 V or 5 V logic levels



A proof of concept Vero Board prototype, was put in service, it ran for many weeks, with reliable performance.



Final Node PCB Version 4.0

PCB was designed with the ability to add other option boards, such as a band pass active filter, with this the placement of the decoupling transformers can be moved from the Node PCB to the option PCB. Should the application not require any transformers, links can be applied to the Node PCB routing the Audio to the outside world.

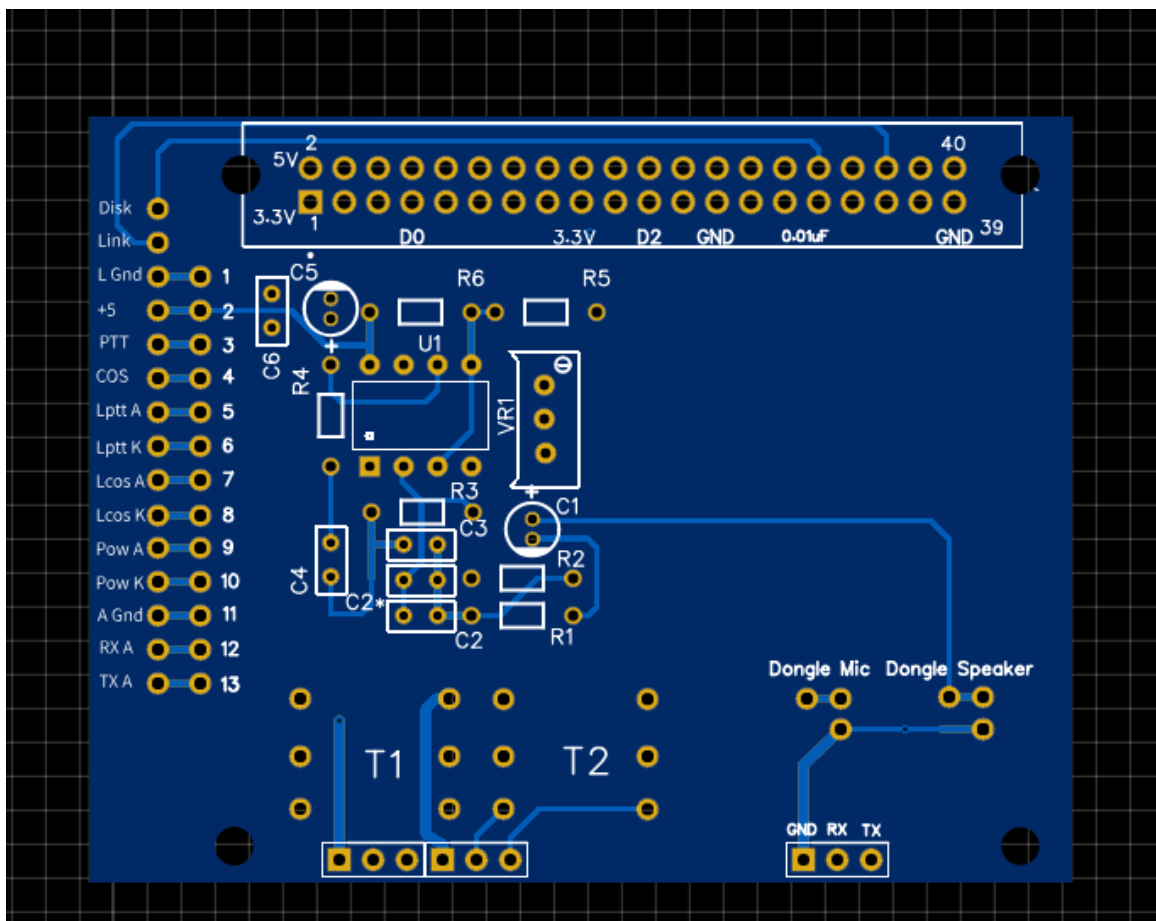
Two option boards had been developed, one is a compressor expander, unfortunately due to extra gain in the circuit, the CPU noise became an issue and this feature has been abandoned.

The second option, a pass band filter to controls the audio from the IP link to the radio, keeping the audio response within 300 Hz to 3 KHz.

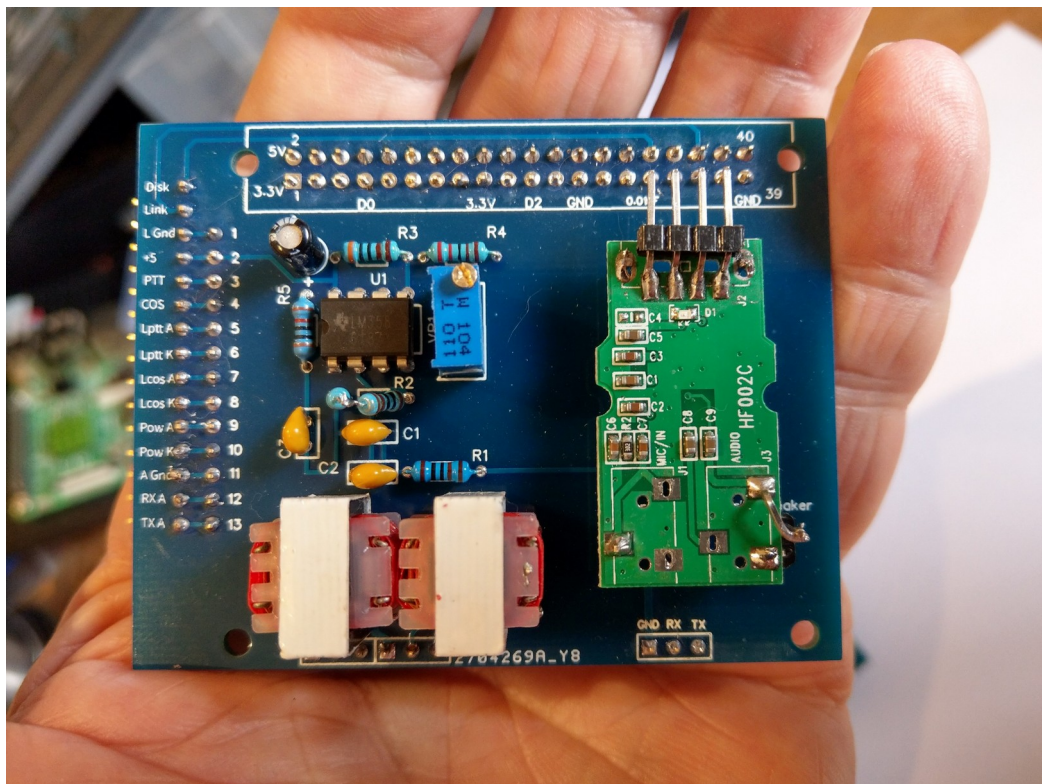
This stops any CTCSS tones that could be present from the IP link going to the Radio transmitter. Note that some radios have built in filters, but not in all cases.

A commercial switch mode power module was used in the final design with a 250 F Super capacitor, the variable shutdown time is done by sensing CPU activity, the super capacitor I used, is way too large for this purpose, a smaller one can be used, as the shut down time of 1 minute is more than enough, however it was cheap compared to others, thus I selected the 250 Farad type

The Audio as is in the original Canadian design, is derived from a USB Sound Dongle, the internals of this dongle are removed from the housing, after removing the audio sockets is used directly by hard wiring to the Raspberry Pi.

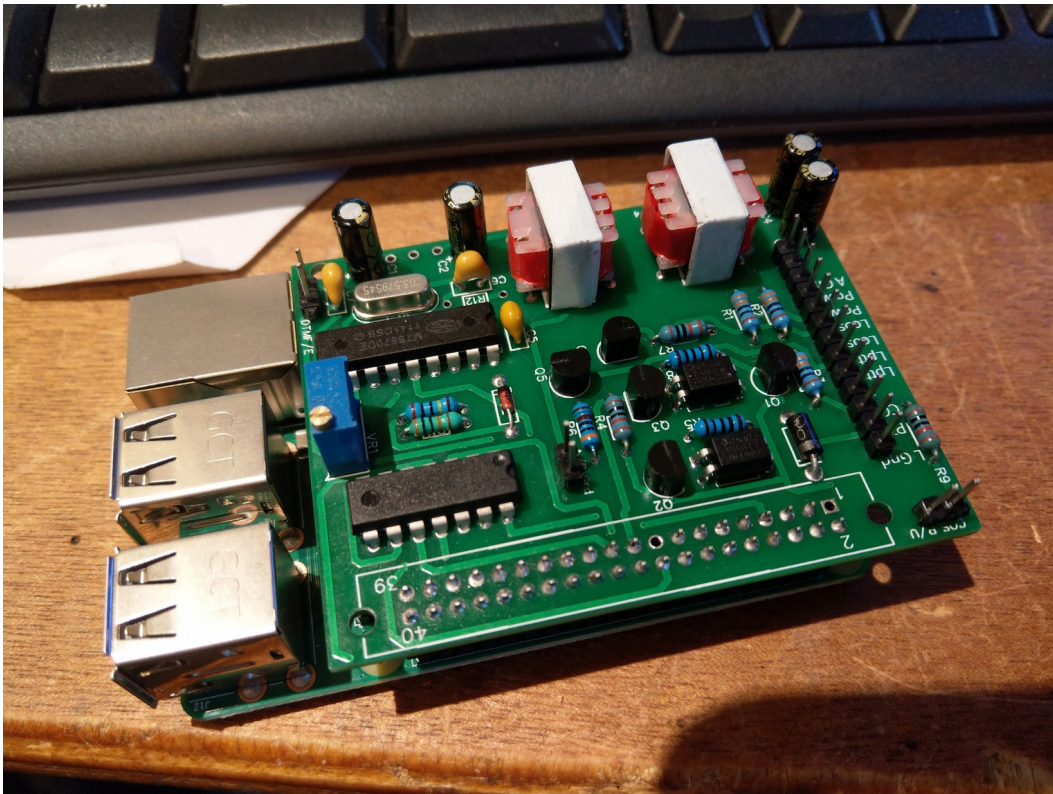


Pass Band Filter PCB

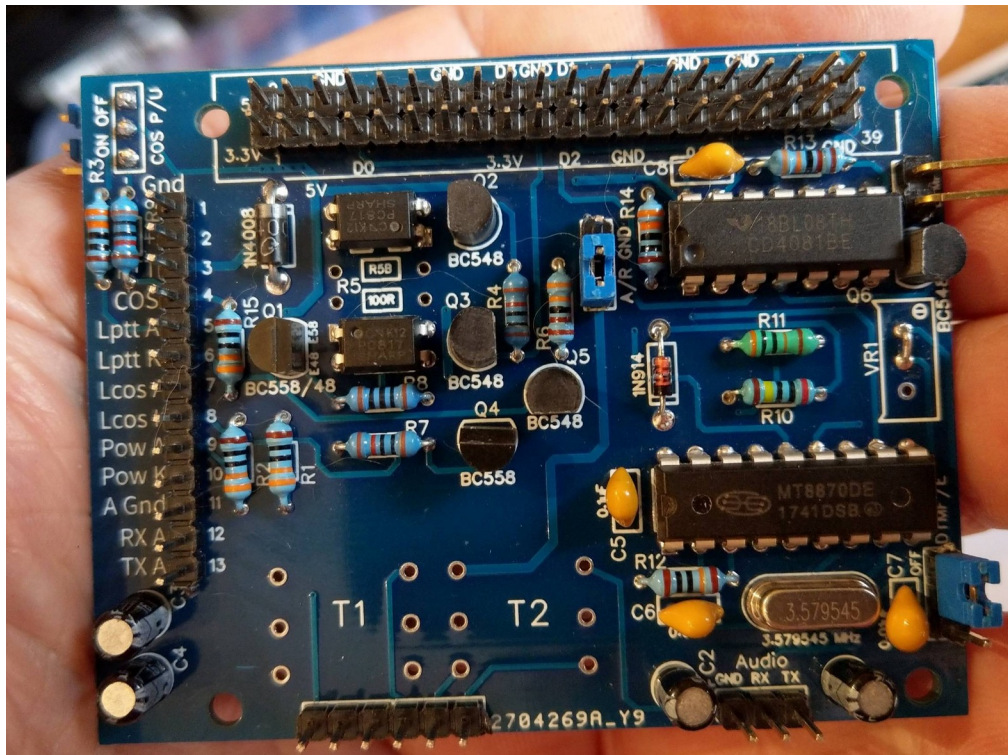


Final Active Pass Band Filter With variable gain & Sound Dongle



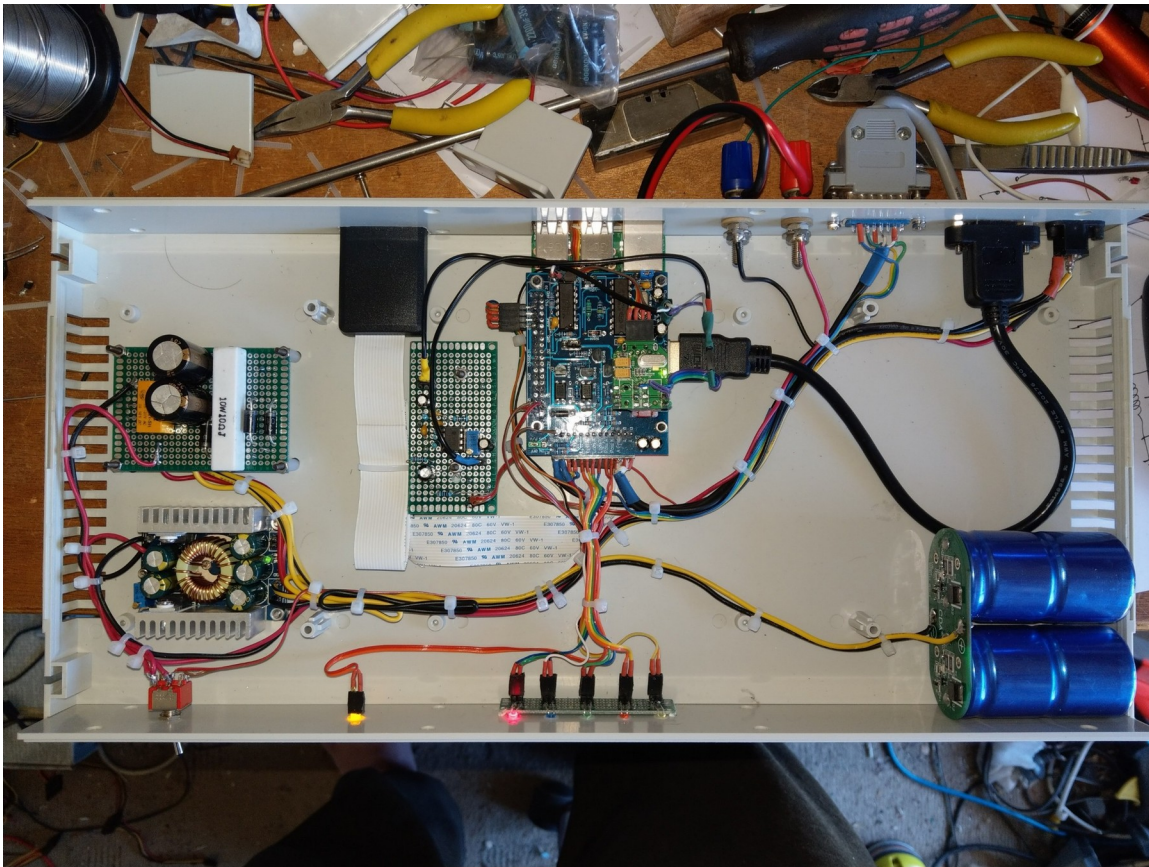


First Production Prototype

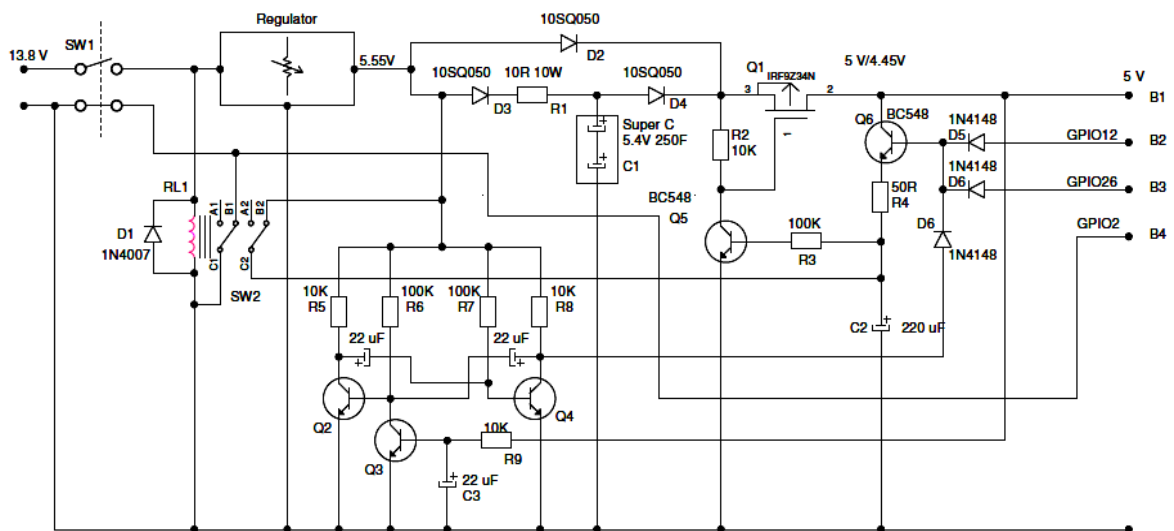


Final Design

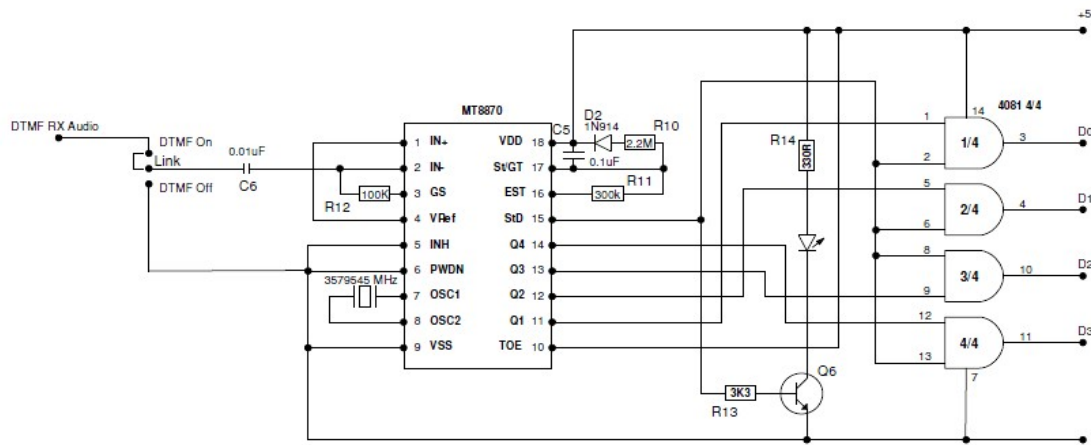




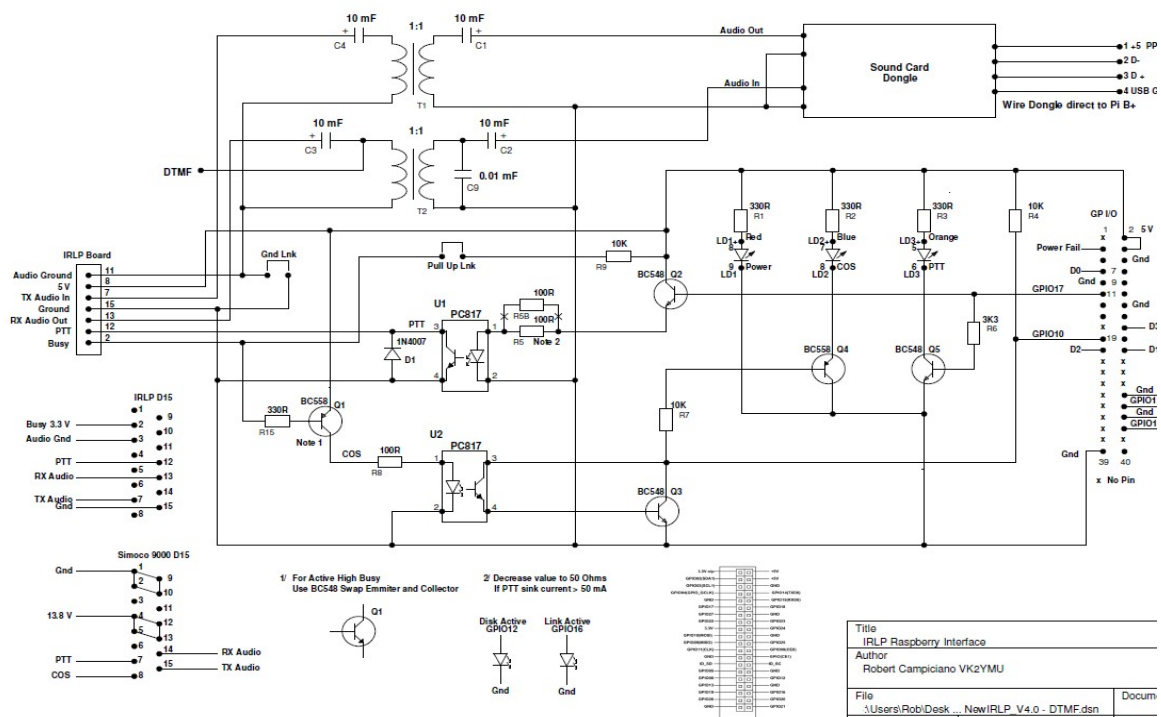
### Prototype showing Switch mode supply with super capacitor



## Power Supply



**DTMF Decoder**



**IRLP Board**

## Radio Control, COS and PTT - IRLP Board

**PTT function** - Upon a high signal from the I/O (GPIO17) 3V Q5 is saturated turning the LD 3 on, The same signal from the I/O turns Q2 on that drives the Opto Coupler U1 to saturate its output pin3 to Logic Low. D1 is protection against PTT Inductive loads, R5 & R5B are to increase the drive current to the Opto Coupler if particular radios require more PTT current sink.

**COS** - Upon reception of a signal the radio will provide a logic low, this turns Q1 on, the output of U2 with Q3 form a darlington configuration, when Q1is turned on, the Opto Coupler is turned on, the collector of Q3 goes Low, turning Q4 on, with LD2 on, this low signal is also fed to the I/O(GPIO10)

The IRLP Board also provides signal from the IRLP software indicating the link to a host to be active.(GPIO16)  
(GPIO12) acts as a memory card access indicator.

**DTMF-** on the IRLP board the DTMF decoder MT8870 with a LED indication of a valid signal, the incoming DTMF tone, provides an output in hexadecimal form (Q1,Q2,Q3,Q4) corresponding to the audio pair of the tones received. The hexadecimal code corresponding to the received tone pair, is applied to the 4081 AND gates. When there is no DTMF signal present, all the outputs (D0 D1,D2,D3) are at Logic 0, this is interpreted by the IRLP software has no code been received. Upon reception of a valid code the StD (pin15) goes to logic High, thus the code representing the received valid tone pair on the Q output of the MT8870 are transferred to the D outputs of the AND gates, the IRLP software detects the presence of a tone and stores that numerical digit waiting for the next digit, when a set of valid numbers are received, the software then takes action. The StD signal is also used to drive the LED by turning Q6 on.

**Audio TX, RX-** The IRLP board is designed to either have the coupling audio transformers in place on the board or placed on another PCB like the optional Band Pass PCB, the kind of radio used for the node, determines if the Band Pass filter is required. Another design feature of the board is that if the coupling transformers are not required they can be linked out with jumpers, completing the audio path to the radio. I tested several USB soundcard dongles, most work well with very minor differences, usually this is the levels that can be adjusted in the IRLP software. To keep the construction compact the internals of these dongles are removed along with the sockets, with direct wiring to the Raspberry Pi.

**Pass Band Filter** - Using an LM358 in a two pole modified Butterworth style filter, R1, R2, C2, C3 forms the filter frequency response elements, Section B is an amplifier with adjustable gain of 100, R5 & R6 are for biasing purposes. This filter purpose is to eliminate any CTCSS tones that could be coming up from the internet, further attenuating any frequencies above 3000 Hz improving the signal to noise ratio. The challenge was to design a narrow pass band with a bandwidth of 2700 Hz with a reasonable flat response across the pass band, with the required rejection to the unwanted frequencies, below 300 Hz, the compromise was to accept a slight lift in the mid range, of the pass band, in practice this has not created any unpleasant results when listening to transmitted audio.

## **Power Supply with Back Up**

### **Power Supply features**

a/ Signal the Raspberry Pi of interruption of main power, causing proper shutdown of all services running in the Raspberry Pi. This interruption can be user initiated or a supply power failure.

b/ Back Up Power for the shutdown process, provided by a super capacitor.

c/ The Power supply can also initiate a boot sequence if there is power but the Raspberry Pi is dormant. This is achieved by sensing a 500mS tick on GPIO26.  
(Requires Software to provide the Tick)

## **Circuit Operation**

**Turn on-** When 13.8 Volts is first applied, SW2(C) normally closed contact, fully charges C2, at the same time Q5 saturates and the gate voltage on the FET goes to 0 Volts, turns on, allowing 5 V on the B1 terminal. At the same time Q3 is saturated, C3 is



fully charged, the astable flip flop is disabled from functioning.

The charge in C2 is maintained by both the tick from GPIO26 or the signal from GPIO12 via Q6

Super Capacitor C1 is charged via D3 and R1, D4 is biased off as the voltage on its cathode is greater than the Anode.

**Power Off or Power fail-** If the input power is removed, RL1 will de-energize, SW2(C) takes B4 to ground, initiating the Raspberry Pi shutdown procedure, D4 turns on and the FET is now supplied with energy from the super capacitor, As long as Q5 is saturated the FET will continue to supply power to the raspberry Pi. Both the Tick and Activity signals keep topping up C2 extending the back up power for as long as required. When both Tick and Activity stop (Raspberry Pi is dormant) and C2 fully discharges, only then will the 5 Volts will be turned off.

**Special Condition-** It is possible to initiate, a power down sequence, with a rapid toggle in the input voltage, the result is having a shutdown when input voltage is still present, in this condition the raspberry Pi will shutdown, not been able to reboot, unless a power cycle is preformed.

Circuitry is include to provide such a power cycle in case of this condition.

Q2 and Q4 form an astable flip flop, this is inhibited by the saturated Q3.

Should C2 fully discharge, turning the FET off, with the presence of input voltage, the astable will cycle once, fully charging C2 and turning the FET back on (Power cycling the Pi) There is an inbuilt delay to when the FET turns off to when its turned back on by the time constant formed by R9 and C3

As a final comment the IRLP image has had code added to it to provide the extra features.

If you wish to implement for example the Power fail system, I will need to patch your SD card with the extra code. This is easily done online

Design and specifications are likely to be changed as this is an ongoing project.

PCB's can be obtained from VK2YMU as are some of the hard to find parts.

The design also lends itself for a private node as it does for repeater use.

Some of the features are not required on a private node.

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My thanks to the following people that contributed to the project in one way or other.

VK3TIM Tim , VK3NA Brad, VK3YNV Ray.

Robert Campiciano

VK2YMU

